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TEM study of the structure of GaAs on vicinal Si(0 0 1) surface grown by MBE

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Molecular beam epitaxy (MBE) grown GaAs films on Si substrates (0 0 1) 4° off towards ⟨1 1 1⟩ A and towards ⟨1 1 1⟩ B, were examined by means of transmission electron microscopy (TEM). The results indicate that in both samples, threading dislocations in the GaAs epilayer are blocked mainly in a thin layer near the GaAs–Si interface. This thin layer is like an inner interface, consisting of pyramidal islands and is flatter on the As growth surface than that on the Ga growth surface. In the type B sample, the density of dislocations is lower, the inner interface is flatter and the number of twins is much larger than that in the type A sample.

1. Introduction

Recently, heteroepitaxial growth of GaAs on Si substrate has received wide attention because of the possible integration of high speed microelectronic and optoelectronic GaAs devices with existing Si circuit technology [1, 2]. However, a high device quality has not been obtained from GaAs based materials directly grown on Si substrates, since the lattice parameter, crystal symmetry, and thermal expansion coefficient of GaAs are different from Si. When GaAs is grown on Si substrate, 4% lattice mismatch between GaAs and Si produces misfit dislocation and twins at the interface. The dislocations propagate from the interface region to the epilayer owing to interaction between misfit dislocation [3]. In order to decrease threading dislocations many methods are adopted, such as a two step growth method [4], annealing [5, 6] and blocking dislocations by superlattices [7]. In addition, antiphase domains may be formed in the GaAs epilayer due to the crystal symmetry. A method for eliminating the antiphase domain was proposed using Si substrates 4° (0 0 1) off towards ⟨1 1 1⟩ to form double atomic layer steps [8]. Furthermore, the difference in thermal expansion coefficients of GaAs from Si substrates places the epilayer under extreme tensile stress and the lattice parameter along the direction parallel to the interface is different from that perpendicular to the interface.

In order to decrease or eliminate the defects in GaAs epilayers, the microstructures of the GaAs–Si heterointerface have been investigated extensively by transmission electron microscopy (TEM). It was shown that there are two types of misfit dislocations in GaAs–Si [9]: 90° and 60° dislocations. It can be considered that the 60° dislocation slides from the growth surface across the {1 1 1} plane or generates at the edge of a growth island; while the 90° dislocation is generated by interaction between two 60° dislocations.

In this paper, the dislocation morphologies and characteristics in GaAs films topped with Ga and As atomic layers grown by molecular beam epitaxy (MBE) are reported, and the effect of growth mechanisms on the defect difference between these two kinds of samples is discussed.

2. Experimental procedure

Epitaxial growth was carried out in a homemade MBE-IV system; Si (0 0 1) 4° off towards ⟨1 1 1⟩ substrates were degreased and etched before loading into the MBE system. A hydrogen passivation layer can be formed on the silicon surface by HF treatment during the etching procedure. After 1000 °C heat treatment, the H layer was desorbed and a clean Si surface was obtained. The growth of a prelayer on the Si surface was monitored by reflection high energy electron diffraction (RHEED). When the substrate temperature ranges between 400 and 600 °C, a 2×1 reconstruction of the surface structure indicates that the prelayer is grown by As and hence the As dimerization axis parallel to the surface step was formed by an As prelayer, or a 1×2 reconstruction originating from the Ga prelayer can be observed.

For comparison, the GaAs films epitaxied on the top of these two prelayers were prepared under the same growth conditions, i.e. by a standard two step growth method. A GaAs buffer layer of 50 nm thickness was first grown at a low substrate temperature of 350 °C, with the growth rate of 0.1 $\mu m h^{-1}$. The RHEED pattern gives direct evidence of the type of epilayers labelled A or B. Type A, where the Ga layer is $2\times$ in the T direction and $4\times$ in the P direction; while type B which is associated with the As layer, is $2\times$ in the P direction and $4\times$ in the T direction. Here T and P represent the directions vertical and parallel to the surface step of Si, respectively. After 600 °C annealing for 5 min, the substrate temperature maintained

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600 °C and the growth rate was then increased to 1 μm h^{-1}. In the second step, a GaAs layer of about 3 μm thickness was grown above type A or B.

The GaAs–Si cross-sectional samples for TEM observation were prepared by sticking two like samples face-to-face with a rotation of 90° to each other and cutting the layer, together with the substrate, into thin slices of about 200 μm thickness along the {1 1 0} plane. The slice were successively thinned by mechanical grinding and ion milling. The final thickness of the observed area was about 100 nm or less. The cross-sectional samples were examined with a H-9000NA electron microscope operated at 300 kV.

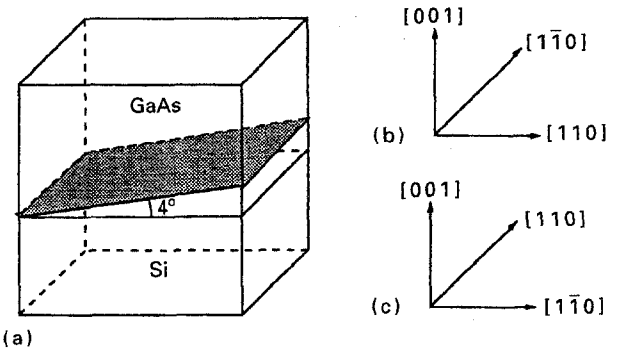

Figure 1 Schematic diagram showing (a) crystal orientation in the GaAs epilayer on the 4° misorientated Si substrate, (b) and (c) are co-ordinate systems for samples of type A and B, respectively.

3. Results and discussion

As the structure of zincblend crystalline GaAs is non-centrosymmetric, the two sets of ⟨1 1 0⟩ direction are

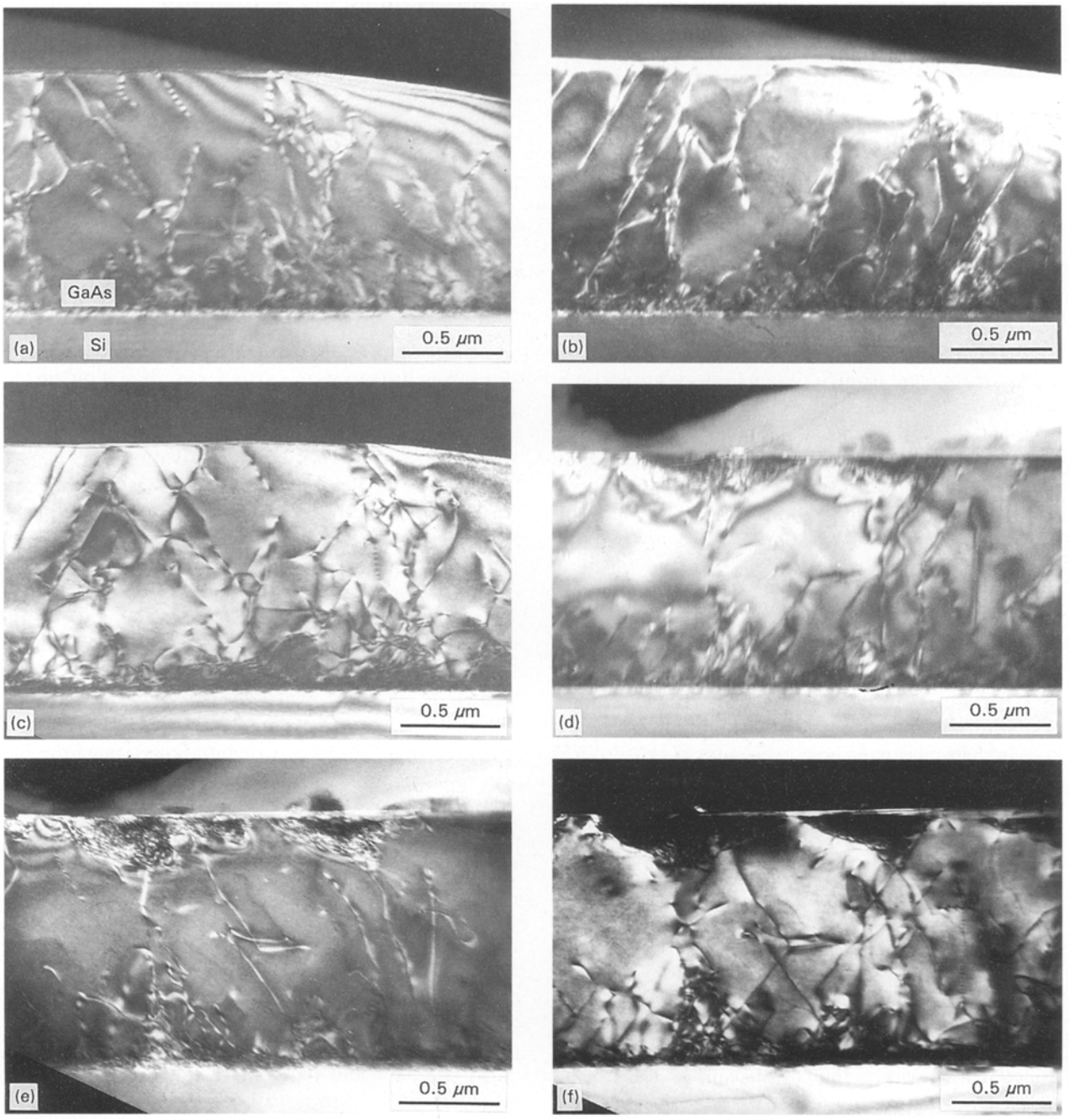

Figure 2 TEM micrographs observed along two orthogonal ⟨1 1 0⟩ directions showing a contrasting change in the defects of type A sample.

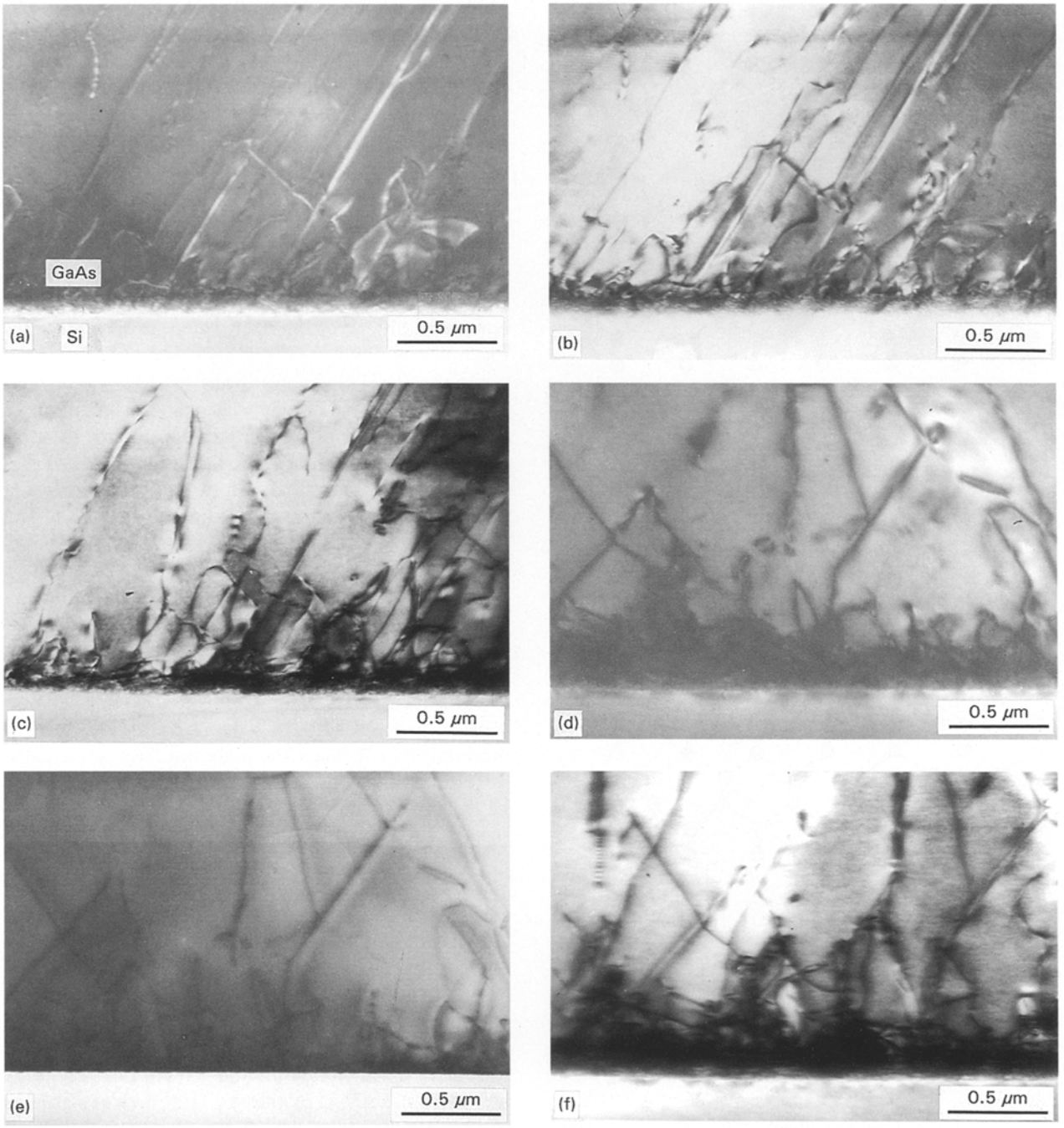

Figure 3 TEM micrographs observed along two orthogonal ⟨1 1 0⟩ directions showing contrasting change in the defects of type B sample.

not equivalent, and the influence of the polarity of such a structure has a significant effect on their crystal growth characters. Since GaAs was epitaxied on a vicinal Si surface, the [1 1 0] and [$\bar{1}$ $\bar{1}$ 0] direction are also not equivalent. Since the Ga growth direction of type A sample is parallel to the surface step of the substrate, while that of type B is vertical to it, if one takes the Ga growth direction of GaAs as the [1 1 0] axis, the tilted direction of the Si substrate is parallel to the [1 1 0] direction in the type A sample and is parallel to [1 $\bar{1}$ 0] for type B sample. This co-ordinate system is shown in Fig. 1.

Since the cross-sectional TEM samples were prepared by sticking the cut slices face-to-face with a rotation of 90° to each other, the GaAs–Si microstructure can be observed along two orthogonal ⟨1 1 0⟩ directions from the same sample. Fig. 2 shows the dislocation structures in sample GaAs–Si of type A. Among the six TEM micrographs, the images in Fig. 2a–c are taken for the same region with the incident beam parallel to the [1 1 0] direction using three different basic vectors $\boldsymbol{g}_{1\bar{1}1}$, $\boldsymbol{g}_{\bar{1}11}$ and $\boldsymbol{g}_{2\bar{2}0}$, respectively; the images in Fig. 2d–f are taken with the incident beam parallel to the [1 $\bar{1}$ 0] direction using three different basic vectors, $\boldsymbol{g}_{11\bar{1}}$, $\boldsymbol{g}_{111}$ and $\boldsymbol{g}_{220}$, respectively. From the contrasting change in threading dislocations in Fig. 2a–c and from the criterion $\boldsymbol{g}\cdot\boldsymbol{b} = 0$, one can determine that most of the dislocations have Burger's vector $\boldsymbol{b}$ of type $\frac{1}{2}$[1 1 0] and $\frac{1}{2}$[0 1 $\bar{1}$]. There are a lot of dislocations blocked at a thin layer near the GaAs–Si interface; this blocking thin layer can be regarded as an inner interface in the GaAs film. Fig. 2c–f shows

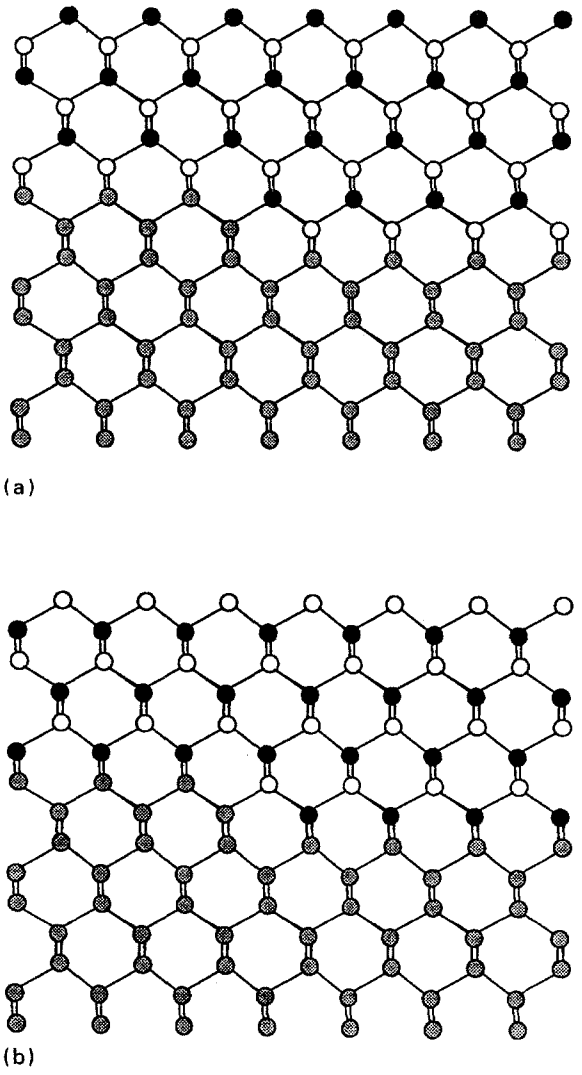

Figure 4 Schematic diagrams showing the growth of GaAs–Si on an atomic scale for samples of (a) type A, and (b) type B: (●) As, (○) (Ga), (◍) Si.

that the GaAs–Si interface consists of a number of islands, and the inner interface in Fig. 2c is flatter than that in Fig. 2f.

Fig. 3 shows the dislocation structures in the type B GaAs–Si sample. The threading dislocations were viewed from both [1 1 0] and [1 $\bar{1}$ 0] directions, such as in Fig. 2. Similarly, the contrasting change of dislocations taken for the same region were compared for three different $\boldsymbol{g}$ vectors. Fig. 3a–c shows images viewed from the [1 1 0] direction using $\boldsymbol{g}_{1\bar{1}1}$, $\boldsymbol{g}_{\bar{1}11}$ and $\boldsymbol{g}_{2\bar{2}0}$, respectively; while Fig. 3d–f shows images viewed from [1 $\bar{1}$ 0] using $\boldsymbol{g}_{11\bar{1}}$, $\boldsymbol{g}_{111}$ and $\boldsymbol{g}_{220}$, respectively. Fig. 3c, f also shows that the GaAs–Si interface consists of a number of islands, and the inner interface in Fig. 3c is flatter than that in Fig. 3f. Comparing Figs 2 and 3, it can be seen that the island structure in Fig. 3 is in general flatter than that in Fig. 2. The density of threading dislocations in Fig. 2 is higher than that in Fig. 3; but there are a lot of twins in Fig. 3, while no twins exist in Fig. 2.

The GaAs cluster formation kinetics have been numerically simulated and studied [10, 11]. It has been shown that pyramidal as well as inverted pyramidal GaAs clusters can be formed with almost equal probability on As terminated Si surfaces. However, the inverted pyramidal clusters grow with a slower rate than pyramidal clusters. The shape of the initial cluster can affect the number of stacking faults (planar dislocations). As one knows, in the initial stage of growth the RHEED patterns show sharp spots and hence the growth surface consists of islands; and, after annealing, the prolonged RHEED spots indicate that the surface becomes flatter than before, so that an inner interface can be generated and the dislocation is blocked at it. Since the mobility of As is higher than that of Ga, the growth surface of As, as well as the corresponding inner interface, is flatter than those for Ga.

On the (0 0 1) plane off towards ⟨1 1 1⟩ A (Ga) face, the step surface is Ga rich, with each Ga having three backbonds and one surface dangling bond. In comparison, the (0 0 1) plane off towards the ⟨1 1 1⟩ B (As) face, has both Ga and As sites; with every three Ga sites corresponding to one As site, and each Ga site has one backbond while each As site has three backbonds (see Fig. 4). Therefore, the (0 0 1) plane tilted towards the ⟨1 1 1⟩ A surface has a higher Ga sticking coefficient than towards the ⟨1 1 1⟩ B face, which yields a larger Ga surface concentration for a given impinging flux value. On the (0 0 1) plane inclined towards the ⟨1 1 1⟩ B surface, it is well established that growth proceeds by the step-terrace-kink growth mechanism [12]. Thus, the inner interface of GaAs–Si (0 0 1) tilted towards ⟨1 1 1⟩ B is flatter than towards ⟨1 1 1⟩ A. The number of pyramids in the interface of type B is less than that of type A.

High resolution electron microscopy (HREM) images show that large terraces on Si substrates and edges of the GaAs island provide sites for microtwin and dislocation nucleation [13]. Thus, one infers that microtwins are generated at edges of high steps. Growth modes are crucial for the presence of the asymmetry. In type A samples, two-dimensional growth maintains the asymmetric terrace steps on the Si substrate, which favours the growth of microtwins on the (1 $\bar{1}$ 1) plane of the ($\bar{1}$ 1 1) and (1 $\bar{1}$ 1) growth planes. In type B samples, as growth planes change to (1 1 1) and ($\bar{1}$ $\bar{1}$ 1) planes and microtwins are generated on these two planes. The nucleation sites due to three-dimensional island growth in type B samples are no longer along the slope of the steps; they are at the edges of islands on the lateral sides of the steps. Hence, there is equal probability for growth of two symmetrically related twins, and the twins can be eliminated by twin intersection.

4. Conclusions

The nature and character of defects generated in MBE grown GaAs films on Si (0 0 1) off towards ⟨1 1 1⟩ A and towards ⟨1 1 1⟩ B have been investigated using diffraction contrast techniques in TEM. Most threading dislocations were confined to a thin layer near the GaAs–Si interface. This thin layer can be treated as an inner interface in the GaAs layer. The GaAs–Si interface consists of pyramidal islands. The inner interface on the As growth surface is flatter than that on the Ga

growth surface. The density of dislocation in the GaAs epilayer grown on the Si (0 0 1) tilted towards ⟨1 1 1⟩ B is less than that towards ⟨1 1 1⟩ A. But there exist a lot of twins in the GaAs epilayer on Si(0 0 1) off towards ⟨1 1 1⟩ B.

References

1. N. OTSUKA, C. CHOI, Y. NAKAMURA, S. NAGAKURA, R. FISHER, C. K. PENG and H. MORKOC, *Appl. Phys. Lett.* **49** (1986) 277.
2. J. B. POSTHILL, J. D. L. TARN, K. DAS, T. P. HUMPHREYS and N. R. PARIKH, *ibid*, **53** (1988) 1207.
3. H. L. TSAI and Y. C. KAO, *J. Appl. Phys.* **67** (1990) 2862.
4. T. C. CHONG and G. FONSTAD, *J. Vac. Sci. Technol.* **B5** (1987) 815.
5. N. CHANG, R. PEOPLE, F. A. BAIOCCHI, K. W. WECHT and A. Y. CHO, *Appl. Phys. Lett.* **49** (1986) 815.
6. L. W. LEE, H. SHICHIJO, H. L. TSAL and R. J. MATYI, *ibid* **50** (1987) 31.
7. N. EL-MASRY, J. C. L. TARN, T. P. HUMPHREYS, N. HAMAGUCHI, N. K. KARAM and S. M. BEDAIR, *ibid.* **51** (1987) 1608.
8. R. FISHER, D. NEUMAN, H. ZABEL, H. MORKOC, C. CHOI and N. OTSUKA, *ibid.* **48** (1986) 1223.
9. S. SHARAN and J. NARAYAN, *J. Appl. Phys.* **66** (1989) 2376.
10. D. K. CHOI, S. M. KOCH, T. TAKAI, T. HALICIOGLU and W. A. TILLER, *J. Vac. Sci. Technol.* **B6** (1988) 1140.
11. S. F. FANG, K. ADOMI, S. LYER, H. MORKOC, H. ZABEL, C. CHOI and N. OTSUKA, *J. Appl. Phys.* **68** (1990) R31.
12. K. F. LONGENBACH and W. I. WANG, *Appl. Phys. Lett.* **59** (1991) 2427.
13. H. L. TSAI and J. MATYI, *ibid.* **55** (1989) 265.

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